IN THE SPECIFICATION

Please replace the paragraph starting at page 35, line 13 with the following:

FIGURE 4 illustrates selected portions of simplified M-ary demodulator 232 in exemplary base station 101 according to an alternate embodiment of the present invention. In the alternate embodiment, only one input processor and only one switch array are used. Input processor 410 stores a snapshot of the M-ary demodulated input signal under command from clock 301A. Demodulation processor 340 loads switch array 411 for the 0 code then directs input processor 410 to send the samples to switch array 411, which routes the signals to WC(0) Accumulator - WC(63) Accumulator according to the settings in switch array 411. The accumulators then process the Logic 0 input signals when strobed by clock 301B. Demodulation processor 340 then loads switch array 411 for the Logic 1 code and directs input processor 410 to send the samples to switch array 411, which routes the signals to WC(0) Accumulator - WC(63) Accumulator according to the settings in switch array 411. The accumulators then process the input 1 signals when strobed by clock 301B. Demodulation processor 340 processor executes these two sequences within the time period of one M-ary modulation symbol bit.